



February 1988

CD4069UBM/CD4069UBC Inverter Circuits

General Description

The CD4069UB consists of six inverter circuits and is manufactured using complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity, and symmetric controlled rise and fall times.

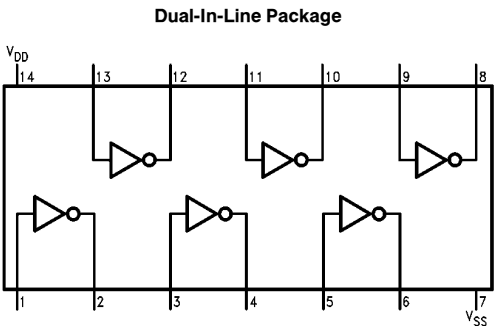
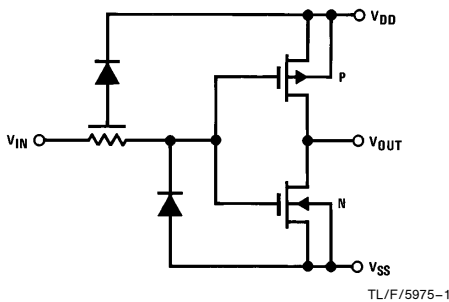
This device is intended for all general purpose inverter applications where the special characteristics of the MM74C901, MM74C903, MM74C907, and CD4049A Hex Inverter/Buffers are not required. In those applications requiring larger noise immunity the MM74C14 or MM74C914 Hex Schmitt Trigger is suggested.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS} .

Features

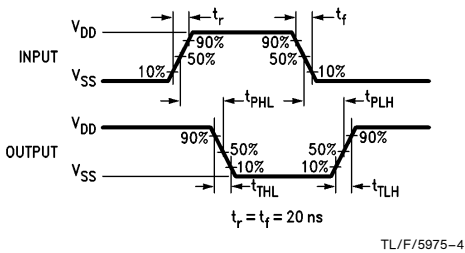
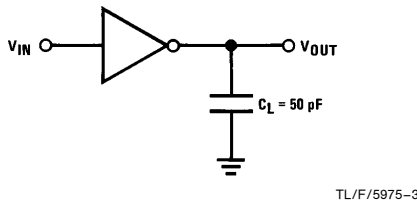
- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} typ.
- Low power TTL compatibility Fan out of 2 driving 74L or 1 driving 74LS
- Equivalent to MM54C04/MM74C04

Schematic and Connection Diagram



Order Number CD4069UB

AC Test Circuits and Switching Time Waveforms



Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD}) $-0.5V$ to $+18 V_{DC}$

Input Voltage (V_{IN}) $-0.5V$ to $V_{DD} + 0.5 V_{DC}$

Storage Temperature Range (T_S) $-65^{\circ}C$ to $+150^{\circ}C$

Power Dissipation (P_D)

Dual-In-Line 700 mW

Small Outline 500 mW

Lead Temperature (T_L)

(Soldering, 10 seconds) $260^{\circ}C$

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})

$3V$ to $15V_{DC}$

Input Voltage (V_{IN})

$0V$ to $V_{DD} V_{DC}$

Operating Temperature Range (T_A)

CD4069UBM

$-55^{\circ}C$ to $+125^{\circ}C$

CD4069UBC

$-40^{\circ}C$ to $+85^{\circ}C$

DC Electrical Characteristics CD4069UBM (Note 2)

Symbol	Parameter	Conditions	$-55^{\circ}C$		$+25^{\circ}C$			$+125^{\circ}C$		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		0.25			0.25		7.5	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		0.5			0.5		15	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		1.0			1.0		30	μA
V_{OL}	Low Level Output Voltage	$ I_O < 1 \mu A$ $V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$ I_O < 1 \mu A$ $V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$ I_O < 1 \mu A$ $V_{DD} = 5V$, $V_O = 4.5V$		1.0			1.0		1.0	V
		$V_{DD} = 10V$, $V_O = 9V$		2.0			2.0		2.0	V
		$V_{DD} = 15V$, $V_O = 13.5V$		3.0			3.0		3.0	V
V_{IH}	High Level Input Voltage	$ I_O < 1 \mu A$ $V_{DD} = 5V$, $V_O = 0.5V$	4.0		4.0			4.0		V
		$V_{DD} = 10V$, $V_O = 1V$	8.0		8.0			8.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$	12.0		12.0			12.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	-4.2		-3.4	-8.8		-2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		-0.10		-10^{-5}	-0.10		-1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4069UBC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I _{DD}	Quiescent Device Current	V _{DD} = 5V, V _{IN} = V _{DD} or V _{SS}		1.0			1.0		7.5	μA
		V _{DD} = 10V, V _{IN} = V _{DD} or V _{SS}		2.0			2.0		15	μA
		V _{DD} = 15V, V _{IN} = V _{DD} or V _{SS}		4.0			4.0		30	μA
V _{OL}	Low Level Output Voltage	I _O < 1 μA								
		V _{DD} = 5V		0.05		0	0.05		0.05	V
		V _{DD} = 10V		0.05		0	0.05		0.05	V
		V _{DD} = 15V		0.05		0	0.05		0.05	V
V _{OH}	High Level Output Voltage	I _O < 1 μA								
		V _{DD} = 5V	4.95		4.95			4.95		V
		V _{DD} = 10V	9.95		9.95			9.95		V
		V _{DD} = 15V	14.95		14.95			14.95		V
V _{IL}	Low Level Input Voltage	I _O < 1 μA								
		V _{DD} = 5V, V _O = 4.5V		1.0			1.0		1.0	V
		V _{DD} = 10V, V _O = 9V		2.0			2.0		2.0	V
		V _{DD} = 15V, V _O = 13.5V		3.0			3.0		3.0	V
V _{IH}	High Level Input Voltage	I _O < 1 μA								
		V _{DD} = 5V, V _O = 0.5V	4.0		4.0			4.0		V
		V _{DD} = 10V, V _O = 1V	8.0		8.0			8.0		V
		V _{DD} = 15V, V _O = 1.5V	12.0		12.0			12.0		V
I _{OL}	Low Level Output Current (Note 3)	V _{DD} = 5V, V _O = 0.4V	0.52		0.44	0.88		0.36		mA
		V _{DD} = 10V, V _O = 0.5V	1.3		1.1	2.25		0.9		mA
		V _{DD} = 15V, V _O = 1.5V	3.6		3.0	8.8		2.4		mA
I _{OH}	High Level Output Current (Note 3)	V _{DD} = 5V, V _O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V _{DD} = 10V, V _O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V _{DD} = 15V, V _O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I _{IN}	Input Current	V _{DD} = 15V, V _{IN} = 0V		−0.30		−10 ^{−5}	−0.30		−1.0	μA
		V _{DD} = 15V, V _{IN} = 15V		0.30		10 ^{−5}	0.30		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, t_r and t_f ≤ 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t _{PHL} or t _{PLH}	Propagation Delay Time from Input to Output	V _{DD} = 5V		50	90	ns
		V _{DD} = 10V		30	60	ns
		V _{DD} = 15V		25	50	ns
t _{THL} or t _{TLH}	Transition Time	V _{DD} = 5V		80	150	ns
		V _{DD} = 10V		50	100	ns
		V _{DD} = 15V		40	80	ns
C _{IN}	Average Input Capacitance	Any Gate		6	15	pF
C _{PD}	Power Dissipation Capacitance	Any Gate (Note 4)		12		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

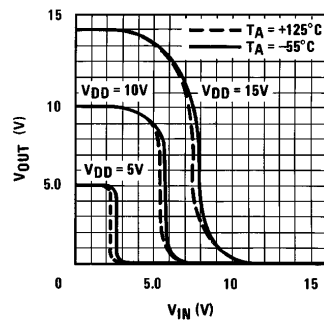
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note—AN-90.

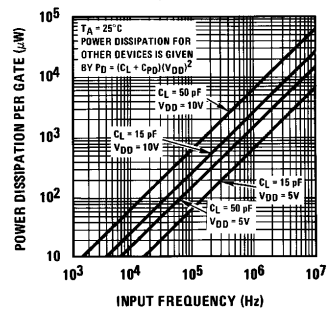
Typical Performance Characteristics

Gate Transfer Characteristics



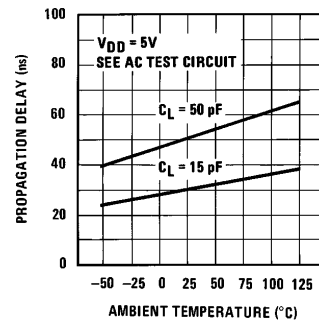
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Power Dissipation vs Frequency



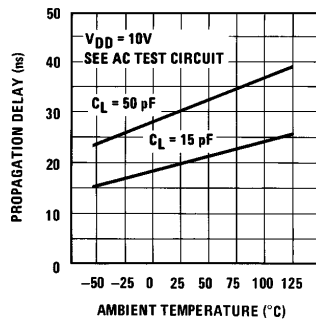
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Propagation Delay vs Ambient Temperature



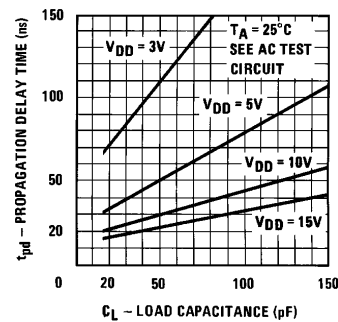
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Propagation Delay vs Ambient Temperature



TL/F/5975-8

Propagation Delay Time vs Load Capacitance



TL/F/5975-9

Physical Dimensions inches (millimeters)

The diagram illustrates the physical dimensions of the CD4069UBMJ/CD4069UBCJ Ceramic Dual-In-Line Package (J) in inches and millimeters. The package is shown from three perspectives: top, side, and end view.

Top View Dimensions:

- Overall width: 0.785 (19.939) MAX
- Pin pitch (between pins 1 and 14): 0.025 (0.635) RAD
- Pin 1 location: 0.220-0.310 (5.588-7.874)
- Pin 14 location: 0.220-0.310 (5.588-7.874)

Side View Dimensions:

- Overall height: 0.180 (4.572) MAX
- Lead angle: 95° ± 5°
- Lead length: 0.310-0.410 (7.874-10.41)
- Lead thickness: 0.008-0.012 (0.203-0.305)
- Lead spacing: 0.098 (2.489) MAX BOTH ENDS

End View Dimensions:

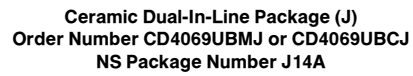
- Overall length: 0.290-0.320 (7.366-8.128)
- Pin pitch (between pins 1 and 14): 0.060 ± 0.005 (1.524 ± 0.127)
- Pin 1 location: 0.018 ± 0.003 (0.457 ± 0.076)
- Pin 14 location: 0.100 ± 0.010 (2.540 ± 0.254)
- Pin 1 thickness: 0.005 (0.127) MIN
- Pin 14 thickness: 0.005 (0.127) MIN
- Pin 1 width: 0.018 ± 0.003 (0.457 ± 0.076)
- Pin 14 width: 0.100 ± 0.010 (2.540 ± 0.254)
- Pin 1 height: 0.125-0.200 (3.175-5.080)
- Pin 14 height: 0.125-0.200 (3.175-5.080)
- Pin 1 length: 0.150 (3.81) MIN
- Pin 14 length: 0.150 (3.81) MIN
- Pin 1 width: 0.018 ± 0.003 (0.457 ± 0.076)
- Pin 14 width: 0.100 ± 0.010 (2.540 ± 0.254)
- Pin 1 height: 0.125-0.200 (3.175-5.080)
- Pin 14 height: 0.125-0.200 (3.175-5.080)
- Pin 1 length: 0.150 (3.81) MIN
- Pin 14 length: 0.150 (3.81) MIN

Other Dimensions:

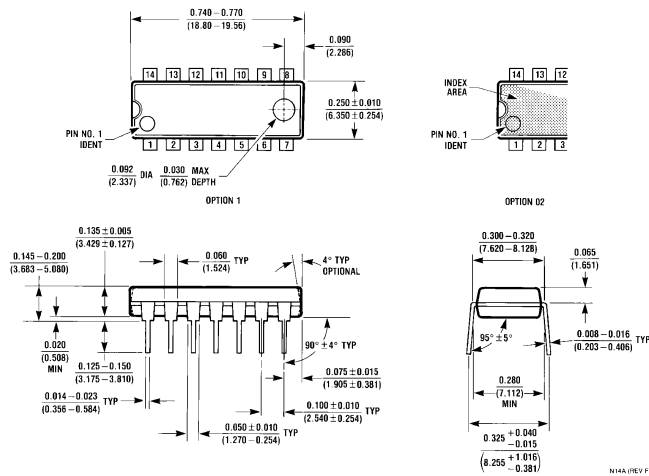
- Lead angle: 86°-94° TYP
- Lead thickness: 0.008-0.012 (0.203-0.305)
- Lead spacing: 0.098 (2.489) MAX BOTH ENDS
- Pin 1 location: 0.018 ± 0.003 (0.457 ± 0.076)
- Pin 14 location: 0.100 ± 0.010 (2.540 ± 0.254)
- Pin 1 thickness: 0.005 (0.127) MIN
- Pin 14 thickness: 0.005 (0.127) MIN
- Pin 1 width: 0.018 ± 0.003 (0.457 ± 0.076)
- Pin 14 width: 0.100 ± 0.010 (2.540 ± 0.254)
- Pin 1 height: 0.125-0.200 (3.175-5.080)
- Pin 14 height: 0.125-0.200 (3.175-5.080)
- Pin 1 length: 0.150 (3.81) MIN
- Pin 14 length: 0.150 (3.81) MIN

Ceramic Dual-In-Line Package (J)
Order Number CD4069UBMJ or CD4069UBCJ
NS Package Number J14A

J14A (REV G)



Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number CD4069UBMN or CD4069UBCN
NS Package Number N14A

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